WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a differential amplifier having a first input coupled to a pad of the integrated circuit and a second input coupled to a reference voltage;

a pull-up transistor coupled between a supply voltage and the pad; and

a logic gate having an output coupled to a control electrode of the pull-up transistor and an input coupled to an output of the differential amplifier.

2. The integrated circuit of claim 1 wherein a voltage output high level at the pad will be the lesser of the reference voltage level or the supply voltage.

3. The integrated circuit of claim 1 wherein the differential amplifier outputs a logic one when a voltage level at the pad is greater than a voltage level of the reference voltage.

4. The integrated circuit of claim 1 wherein the reference voltage is less than the supply voltage.

5. The integrated circuit of claim 1 further comprising:

a leaker device coupled to the pad to statically hold the pad at a desired VOH level or above.

6. The integrated circuit of claim 5 wherein a control electrode of the leaker device is coupled to a leaker reference voltage which is generated on-chip.

7. The integrated circuit of claim 5 wherein a control electrode of the leaker device is coupled to a supply voltage.

8. The integrated circuit of claim 1 further comprising:

a voltage reference generator circuit, coupled to the second input of the differential amplifier, to generate the reference voltage.

9. The integrated circuit of claim 1 wherein the reference voltage is provided by way of an external source coupled to a pad of the integrated circuit.

10. The integrated circuit of claim 1 wherein the logic gate performs an OR function.

11. The integrated circuit of claim 1 further comprising:

logic array blocks, configurable to implement user-logic functions, providing a logical output coupled to another input of the logic gate.

12. The integrated circuit of claim 1 wherein the pad is also coupled to an input buffer circuit.

13. The integrated circuit of claim 8 wherein the voltage reference generator is programmable to select a level of the reference voltage.

14. The integrated circuit of claim 8 wherein the voltage reference generator is programmed before the integrated circuit is used for normal operation.

15. The integrated circuit of claim 8 wherein the voltage reference generator is programmable to select from a plurality of reference voltage levels.

16. The integrated circuit of claim 1 wherein the supply voltage is a noisy VCC supply voltage.

17. The integrated circuit of claim 1 wherein the integrated circuit is a programmable logic integrated circuit.

18. The integrated circuit of claim 1 wherein the pull-up transistor dynamically holds the pad at a voltage output high level.

19. The integrated circuit of claim 1 further comprising:

a standard I/O buffer circuit coupled to the pad, wherein the standard I/O buffer circuit provides support for voltage output high levels compatible with the supply voltage, and the pull-up transistor, differential amplifier, and logic gate provide support for voltage output high levels compatible with voltages other than the supply voltage.

20. The integrated circuit of claim 1 wherein the pull-up transistor is a PMOS device.